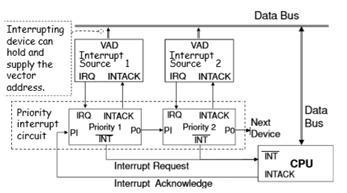
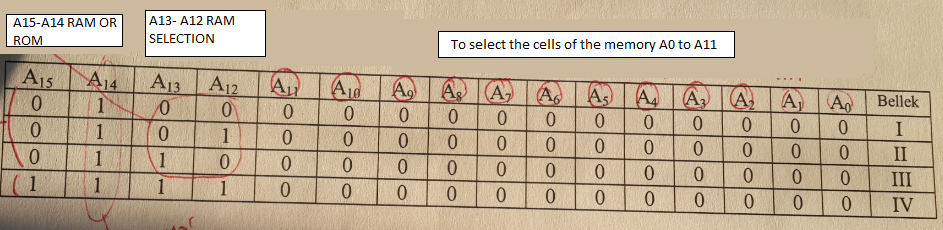
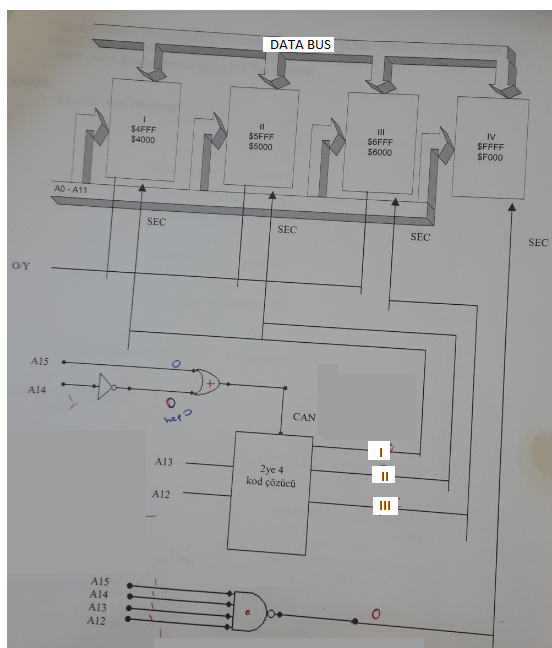
SORU1: Draw a daisy chain which has 2 cell. The I/O devices has their own VAD. Design the connections between daisy chain, I/O device and CPU.



SORU 2: The CPU has 16 bits adress bus and 8 bits data bus. Design memory that includes 3 4K x8 RAM and one 4Kx8 ROM. Locate the RAM starting from $4000 memory adress. And locate the ROM starting from the $F000 memory adress. The connection between CPU and memory is asyncronous communication. Design the connections between CPU and memory.





You can use or gate to select each RAM instead of using a decoder.

For example for selecting RAM-I: A15:0, A14:1, A13:0 and A12:0 if these values are like these; the CPU selects first RAM to communicate. The following gate is a or gate.

Chip select of the first RAM should be (CS= A12 or A13 or A14’ or A15)

A12

A13

CS

+

A14

A15

If A15:0, A14:1, A13:0 and A12:1 , the second RAM will be selected. You should define CS for each memory.